# Field-Programmable Gate Array Development Cycle

HCDC LLC
HIGH-TECH CONSULTING
for DIGITAL COMMUNICATIONS

## Laboratory Misson

The main purpose of an FPGA Laboratory is to address research and development issues in the rapid transition of signal processing alogrithms into functional hardware prototypes. We concentrate on computational issues and hardware-specific designs of algorithms.

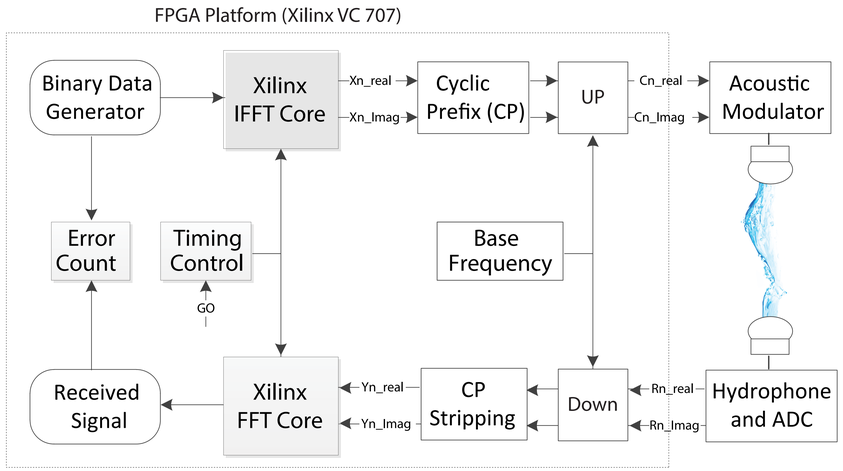
**Key Applications Areas Are:**

- Digital communications algorithms for acoustic underwater communications;
- Joint detection algorithms for satellite and land-mobile radio channel;
- Intermediate and support implementation for ultimate low-power VLSI circuits.

**OFDM Transmitter for acoustic communications (UW-OFDM)**

Orthogonal Frequency-Division Multiplexing (OFDM) has recently been applied to underwater communications. OFDM offers a number of advantages, in particular it facilitates equalization on channels with large delay spreads.

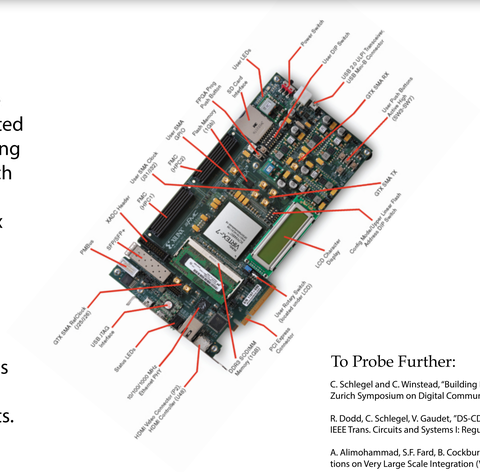
However the rapid time variations of the medium cause inter-channel interference (ICI), which needs to be equalized..



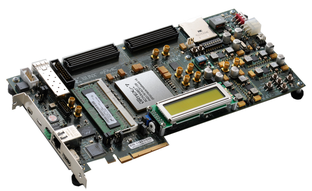

## Why FPGAs?

Field-Programmable Gate Arrays are generalized very large-scale integrated circuits which can be configured using hardware description languages such as VHDL and Verilog. This allows for rapid prototyping of highly complex communications algorithms with a significantly reduced effort both in terms of manpower and cost.

FPGAs are increasingly used in industry not only to build prototypes but also produce actual products, especially in small or custom projects.



The Xilinx Virtex VC 707 test bench contains the most advanced Xilinx FPGA chip XC7VX485T with 2 millon logic cells, DSP, on-board memory, and support circuits, fabricated in the 28nm processing node.



To Probe Further:

C. Schlegel and C. Winstead, "Building Energy-Efficient Error Control Decoders: What are the practial limits?", International Zurich Symposium on Digital Communications, Zurich, February 2014.

R. Dodd, C. Schlegel, V. Gaudet, "DS-CDMA Implementation With Iterative Multiple Access Interference Cancellation," IEEE Trans. Circuits and Systems I: Regular Papers, Vol. 60, No. 1 pp. 222- 231, 2013.

A. Alimohammad, S.F. Fard, B. Cockburn, C. Schlege, "A Compact and Accurate Gaussian Variate Generator," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol, 16, No.: 5, pp. 517- 527 , 2008.

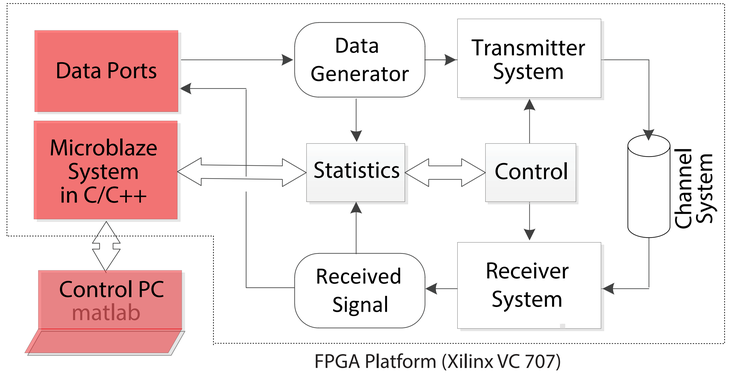
## Modern FPGA Workstation

**Typcal Design Flow:**

**FPGA Systems** are programmed in VHDL or Verilog and put onto FPGA testboards.

**Data Monitoring and Control** are executed from a PC via the Xilinx embedded Microblaze RISK processor, which communicates via control ports, UART, Ethernet

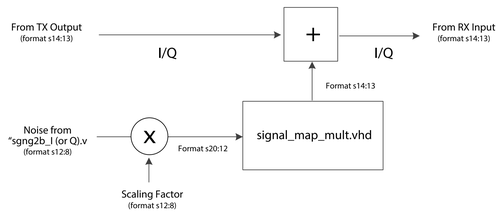
**Data Processing** is carried out through the data ports of the board, such as Ethernet, USB




## FPGA Cores

FPGA projects are typically built from individual pieces, called cores. These cores can then be assembled into complete sub-systems and systems. An example core we developed is used to simulate noise, white Gaussian noise in particular.

This module has a very simple mathematical description **Additive White Gaussian Noise Channel (AWGN) module :**

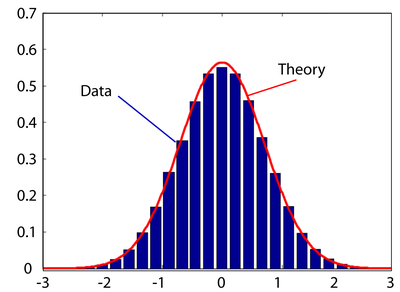



**Purpose:**

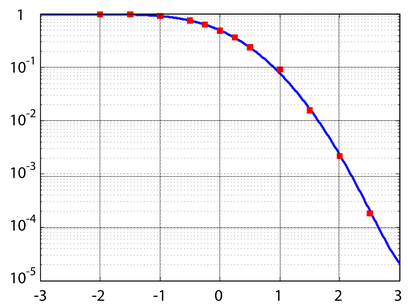
1. Acceleration of the transition from algorithms to hardware
2. Development of R&D prototypes to rapidly establish feasibilty of systems components and hardware requirements
3. Implementation of Advanced Communications Algorithms to verify theoretical research results
4. Rapid transition of research into product applications

**Experimental Verification**

Experiments with the hardware are conducted to verify that the core agrees with theory:




- Historgram for 0dB noise




- Tail distribution for 0dB noise: Sliced error probability